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Silicon-based Fin Field-Effect Transistor (Si-FinFET) Optimisation Based on Gate Length and Operating Temperature

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ABSTRACT

This study provides an in-depth investigation into the temperature sensitivity of Silicon-based Fin Field-Effect Transistor (Si-FinFET), highlighting their viability as nano-dimensional temperature sensors. The Multi-Gate Field-Effect Transistor (MuGFET) simulation framework was utilised to model and analyse the thermal response characteristics of Si-FinFET structures. Simulations of the current voltage (I-V) profiles were conducted across a range of temperatures and gate lengths (L_g = 10, 20, and 30 nm), with the temperature sensitivity quantified under a diode-mode operational scheme. The optimum sensitivity was identified through the maximum differential current (ΔI) within the supply voltage window (V_{DD} = 0-1 V). Notably, a linear augmentation in temperature sensitivity was observed as the channel length increased from 10 nm to 20 nm, underscoring the scalability and enhanced thermal responsivity of Si-FinFET architectures for advanced nanoscale sensing applications.

Keywords: Channel length, FinFETs, nano sensor, Si, temperature

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INTRODUCTION

In the realm of modern nanoelectronics, device-level thermal sensing has become increasingly indispensable for ensuring system reliability, particularly as integrated circuits operate under escalating power densities and aggressively scaled geometries. As conventional Metal Oxide Field-Effect Transistor (MOSFET) technologies approach their fundamental

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scaling limits, research attention has pivoted toward next-generation Field-Effect Transistor (FET) architecture. Among these, the Fin Field-Effect Transistor (FinFET) has emerged as a preeminent candidate, offering enhanced electrostatic control, mitigation of short-channel effects, and seamless compatibility with nanoscale fabrication processes. FinFETs have been extensively investigated across both academic and industrial platforms for their applications in logic circuits, memory architectures, and, more recently, as promising candidates for sensing technologies. Building upon this foundation, the present study explores the temperature-dependent electrical behaviour of silicon-based FinFET (Si-FinFET) and critically evaluates their feasibility as nanoscale thermal sensors (Ariga et al., 2014; Liu et al., 2015; Lu et al., 2015; Yu et al., 2022). The geometrical structure of Si-FinFET is shown in Figure 1.

Semiconductor-based temperature sensors represent quintessential examples of embedded sensing devices within electronic systems (Meijer et al., 2001). In such configurations, the current voltage (I-V) characteristics of nanowire transistors form the cornerstone for the development of transistor-based thermal sensors (Doghish & Ho, 1992; Hashim & Sidek, 2011, 2012; Kesherwani et al., 2022; Liao et al., 1999). Notably, a Bipolar Junction Transistor (BJT) can function as a temperature sensor by shorting its base and collector terminals, effectively operating in diode mode. Similarly, in MOSFET-based designs, the gate terminal may be interconnected with either the source or drain to facilitate thermal sensing functionalities, as depicted schematically in Figure 2. The miniaturisation of fundamental electronic components such as capacitors, diodes, resistors, and transistors at the nanoscale has further catalysed their widespread adoption within the modern electronics industry.

The efficacy of emerging nanoelectronic technologies is intrinsically tied to their nanoscale dimensional attributes. As advancements in fabrication and modelling continue, the integration of ultra-miniaturised transistors into system-on-chip architectures is poised to enhance device reliability and functionality. Despite the well-recognised scaling bottlenecks of traditional MOSFET structures, innovations in nano-scaled FET architectures remain revolutionary, necessitating continued exploration through novel modelling techniques and technological ingenuity to circumvent existing physical limitations.

Simulation methodologies have become indispensable for augmenting experimental efforts in the characterisation and optimisation of nanoscale MOSFETs (Bescond et al., 2004). Beyond device fabrication, simulation techniques enable the evaluation of structural advantages and trade-offs, cost-efficiency projections, and scalability potential for MOSFETs operating in the nanometer regime (Alvarado et al., 2013; Dixit et al., 2019; Fahad et al., 2015; Jaisawal et al., 2022; Li et al., 2021).

The FinFET architecture incorporates a diverse selection of semiconductor materials, including silicon (Si), germanium (Ge), gallium arsenide (GaAs), and indium arsenide

(InAs), each imparting distinct electronic properties that critically influence FinFET performance metrics (Hashim, 2017). This research focuses on the comprehensive analysis of temperature sensitivity and thermal stability in Si-FinFET devices operating under diode-mode configurations. Emphasis is placed on assessing the impact of varying Si channel lengths and operational temperature ranges on pivotal electrical parameters, such as drain-induced barrier lowering (DIBL), threshold voltage (V_T), and sub-threshold swing (SS). Through this investigation, the study aims to elucidate the potential of Si-FinFET-based structures as highly responsive nanoscale thermal sensors.

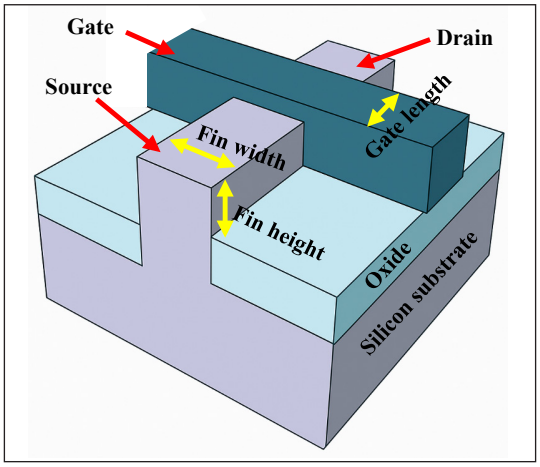

Figure 1. Geometrical structure of Si-FinFET

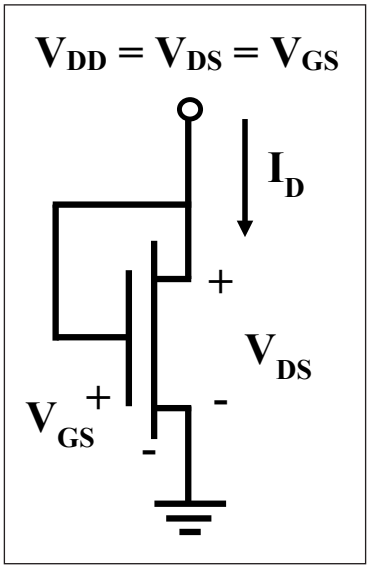

Figure 2. Diode connection mode of MOSFET as a temperature sensor

RESEARCH METHOD

This study systematically examines the performance characteristics of Si-FinFET transistors using the MuGFET modelling tool. The output I-V characteristic curves are simulated under a range of operational conditions and device configurations. These simulation-derived I–V characteristics are subsequently analysed to investigate the influence of key parameters, such as temperature and gate length, on the electrical behaviour of nanowire transistors. Specifically, Purdue University's MuGFET simulation platform (Park et al., 2021) is employed, renowned for its accuracy in modelling nanometer-scale multigate FET architectures.

MuGFET incorporates simulation frameworks originally developed at Bell Laboratories, namely PADRE and PROPHET. PADRE serves as a device-oriented simulator capable of modelling structures in one, two, or three dimensions with complex, variable geometries, while PROPHET functions as a partial differential equation (PDE) solver that supports one-, two-, and three-dimensional profiling (Jabbara et al., 2022; Nasri et al., 2023; Park et al., 2021). By offering robust and physically consistent solutions, MuGFET enables researchers to generate reliable FET output characteristics, particularly when detailed physical modelling of carrier transport phenomena is required. It solves the Poisson and drift-diffusion equations self-consistently, thereby facilitating the precise simulation of nanoscale transport behaviour (Ahangari et al., 2022; Hashim, 2022a).

The MuGFET tool, available via Purdue University's nanoHUB platform, has become a benchmark in the field of nanoelectronic device modelling. It specifically targets the simulation of nanoscale multigate FET structures, such as FinFETs and nanowire transistors, using drift-diffusion-based approaches. Given the prohibitive fabrication costs and sensitivity of nanodevices, simulation-driven design using MuGFET has emerged as a crucial strategy for minimising experimental losses and optimising device architectures (Atalla et al., 2019, 2020, 2023; Das et al., 2018; Hashim, 2022a; Kumar et al., 2020).

To accurately reproduce the transfer characteristics (I_d-V_g) of Si-FinFETs at varying temperatures, the MuGFET simulations utilise a set of carefully selected parameters, including the doping concentrations of the channel (P-type) and source/drain regions (N-type), channel width, source/drain lengths, and gate length. Of particular interest are the oxide thickness and gate length, both critical determinants of device scaling behaviour. Figure 3 depicts a representative Si-FinFET simulation environment (Mehrdad et al., 2022; Nasri et al., 2022).

For this investigation, the I_d-V_g characteristics were simulated at temperatures of 275 K, 300 K, 325 K, and 350 K, across gate lengths (L_g) of 10 nm, 20 nm, and 30 nm. The oxide thickness was fixed at 1 nm, with source and drain lengths set at 5 nm each. Both the source and drain regions were uniformly doped as N-type, while the channel width was maintained at 10 nm with a doping concentration of 10^{19} cm^{-3}.

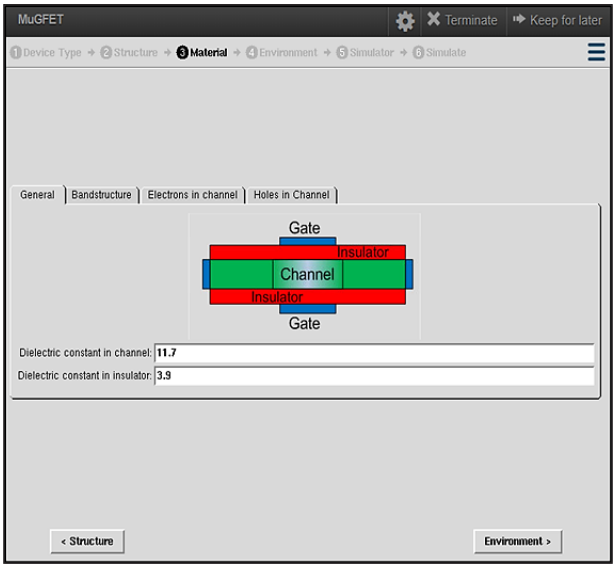

Figure 3. Homepage of MuGFET simulation tool

RESULTS AND DISCUSSION

The variation in output current (ΔI) for gate lengths (L_g) of 10, 20, and 30 nm at a fixed gate width (W_g) of 10nm is illustrated in Figures 4 through 6 as a function of temperature, with the supply voltage (V_{DD}) swept from 0 to 1 V in 0.1 V increments. The graphs clearly exhibit a linear decline in current with increasing temperature across all V_{DD} values, indicating a strong inverse temperature dependence. Notably, the peak temperature sensitivity, represented by the maximum current response, is observed at relatively lower temperatures. Figures 4 and 5 highlight that the highest temperature sensitivity occurs at V_{DD} = 0.6 V for both L_g = 10 nm and L_g = 20 nm, respectively, whereas Figure 6 reveals a comparatively lower response for L_g = 30 nm under the same biasing condition. These findings collectively underscore that V_{DD} = 0.6 V represents an optimal operating point for Si-FinFET thermal sensing, providing stable and maximised sensitivity within the critical temperature window of 325-350 K.

The variations in ΔI with decreasing V_{DD} at temperatures of 275 K, 300 K, 325 K, and 350 K for L_g of 10, 20, and 30 nm are depicted in Figures 7 through 9. The highest temperature sensitivity, represented by the peak ΔI, was observed at V_{DD} = 0.1 V for L_g = 10 nm, V_{DD} = 0.3 V for L_g = 20 nm, and V_{DD} = 0.4 V for L_g = 30 nm. These findings indicate that ΔI am strongly dependent on both increasing temperature and V_{DD}, with an optimum operating condition identified at V_{DD} = 0.4 V, L_g = 30 nm, and W_g = 10 nm.

To elucidate the sensing performance more comprehensively, temperature sensitivity was evaluated by analysing the slope of the ΔI–T characteristics across different gate lengths.

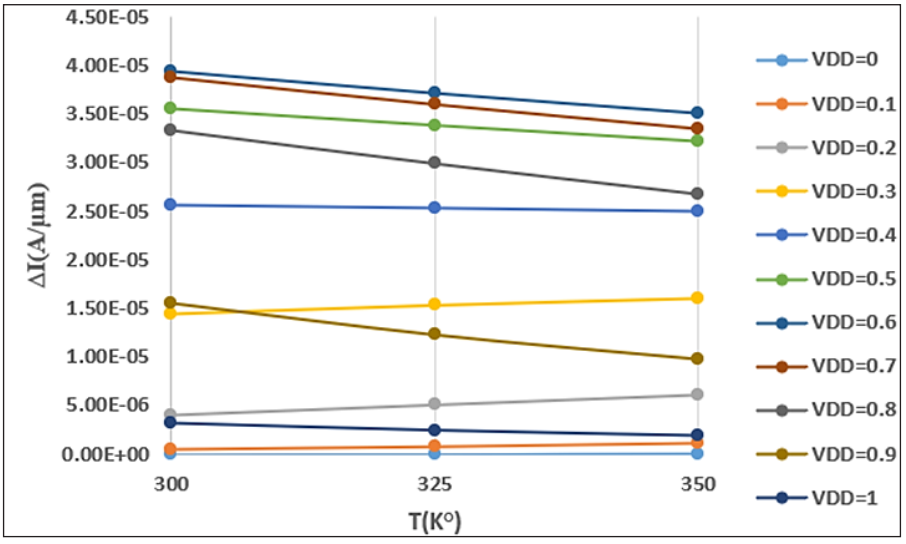

Figure 4. ΔI–T characteristics of Si-FinFET (W_g=10nm, L_g = 10nm)

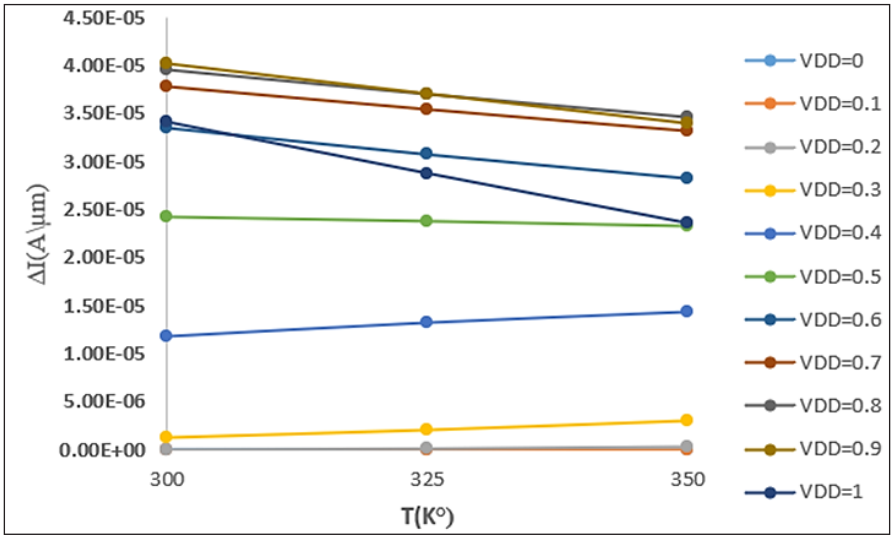

Figure 5. ΔI–T characteristics of Si-FinFET (W_g =10nm, L_g=20nm)

The results clearly reveal that shorter gate lengths, particularly L_g = 10 nm, exhibit a steeper slope, signifying an enhanced response to temperature fluctuations and superior thermal sensitivity. Conversely, as the gate length increases, the ΔI-T curves display a more subdued gradient, indicating diminished sensitivity. This trend underscores the pivotal influence of channel length on the thermal responsiveness of Si-FinFET-based nanoscale temperature sensors, affirming the strategic advantage of ultra-scaled devices in high-precision thermal sensing applications.

Figure 10 highlights the optimal operating voltage (V_{DD}) correlated with the temperature sensitivity peaks identified in Figures 7 to 9, based on variations in channel length and thermal responsiveness. Although the channel length increases only incrementally from 10 to 30 nm, a marked enhancement in temperature sensitivity is observed at L_g = 10 nm. Beyond this, a quasi-linear decline in sensitivity is noted as the gate length extends from 10 to 20 nm and further to 30 nm. These observations confirm that the most favourable dimensional configurations for thermal sensitivity are attained at L_g = 10 nm and L_g = 20 nm.

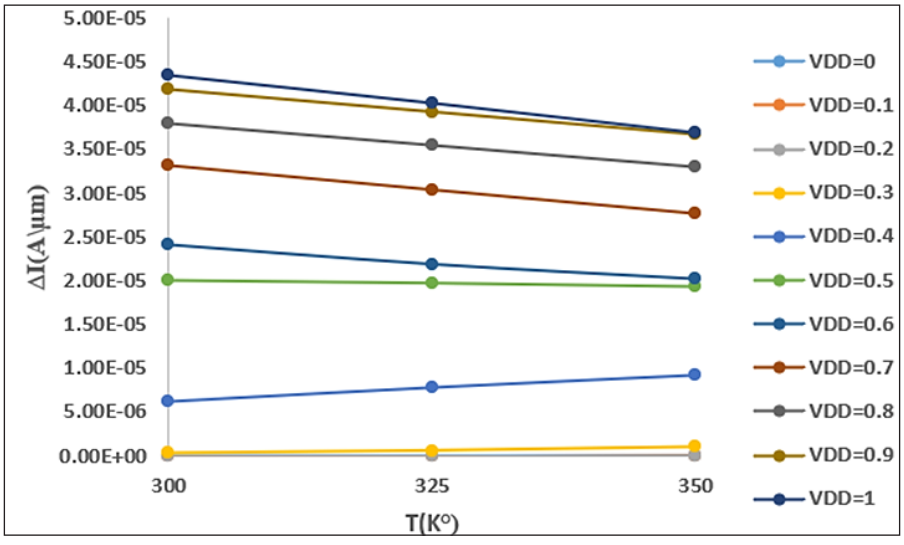

Figure 6. ΔI–T characteristics of Si-FinFET (W_g=10nm, L_g=30 nm)

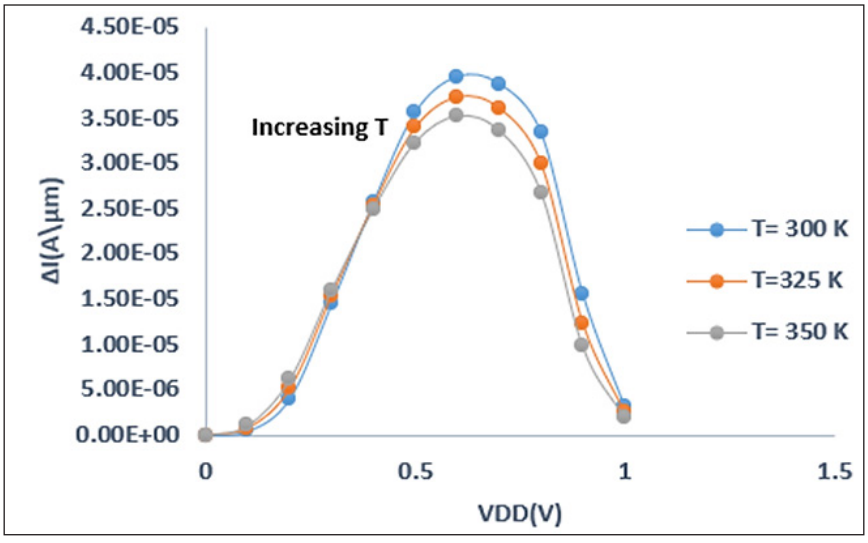

Figure 7. ΔI–V_{DD} characteristics of Si-FinFET (W_g=10nm/ L_g = 10nm)

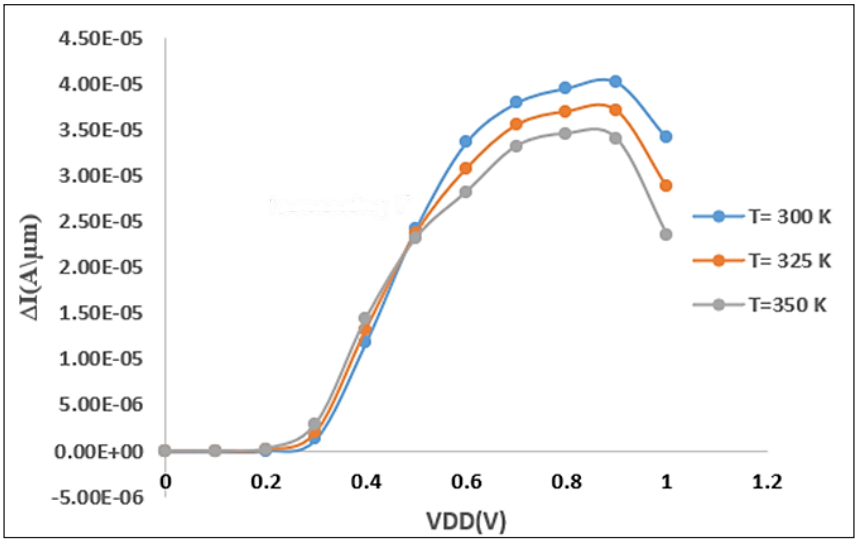

Figure 8. ΔI–V_{DD} characteristics of Si-FinFET (W_g=10nm, L_g = 20nm)

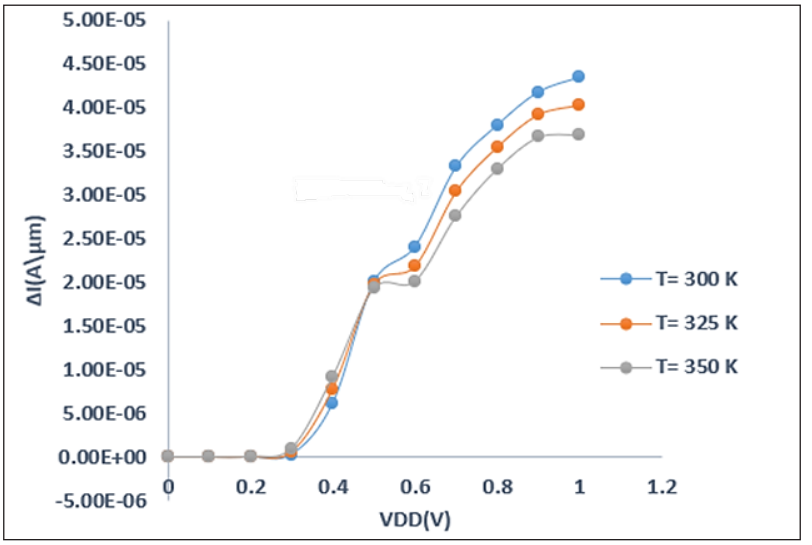

Figure 9. ΔI–V_{DD} characteristics of Si-FinFET (W_g = 10 nm, L_g = 30 nm)

The consolidated results presented across Figures 4 to 10 reveal a definitive trend in the temperature-dependent current behaviour of Si-FinFETs. Specifically, increasing temperature consistently induces a monotonic reduction in ΔI, attributed to intensified phonon scattering that degrades carrier mobility. However, the magnitude of this thermal response, quantified as the slope of the ΔI–T characteristic, varies with gate length, with L_g = 10 nm exhibiting the most pronounced sensitivity.

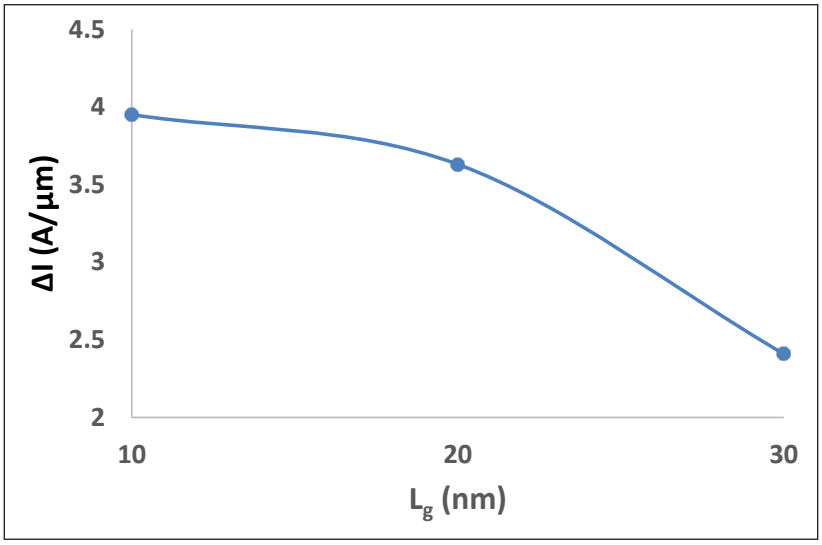

Figure 10. ΔI variation with channel length (L_g) for optimal temperature sensitivity and V_{DD} tuning

This can be ascribed to the amplified electric field intensity and stronger confinement effects within ultra-scaled channels, which intensify temperature-dependent modulation.

Additionally, the relationship between ΔI and V_{DD}, as illustrated in Figures 7 to 9, demonstrates a nonlinear dependency wherein a moderate bias range ($V_{DD} \approx 0.3–0.6$ V) produces maximal ΔI. Beyond this optimal biasing window, the current saturates, suggesting diminishing returns in sensor performance at higher voltages. Figure 10 effectively consolidates these findings by delineating the precise combinations of gate length and supply voltage that yield peak temperature sensitivity. The observed near-linear attenuation of ΔI with increasing gate length reinforces the conclusion that ultra-scaled Si-FinFETs are inherently more responsive to temperature variations, albeit with trade-offs concerning leakage currents and electrostatic control. These insights are instrumental in the strategic optimisation of Si-FinFET-based nanoscale thermal sensors, offering valuable design guidance on the selection of geometrical and electrical parameters to achieve a judicious balance between high thermal sensitivity and device stability.

Figure 11 presents the temperature-dependent behaviour of key performance parameters in Si-FinFETs, namely, drain-induced barrier lowering (DIBL), subthreshold swing (SS), and threshold voltage (V_T), measured at temperatures of 275 K, 300 K, 325 K, and 350 K with a gate length (L_g) of 10 nm. A clear linear decline in V_T is observed as the temperature increases: for instance, V_T drops from 0.28 V at 275 K to 0.22 V at 350 K, indicative of thermally induced carrier activation and reduced threshold control.

The SS, which ideally approaches 69.5 mV/dec, starts at 120.39 mV/dec at 275 K and progressively increases, peaking at 161.63 mV/dec at 350 K, highlighting the degradation in

gate control over the channel at elevated temperatures. Notably, this deviation underscores the sensitivity of SS to thermally induced interface trap states and leakage current contributions. Additionally, DIBL exhibits a monotonic increase with temperature, further confirming the deterioration of electrostatic integrity under thermal stress.

Overall, these findings reveal that as ambient temperature rises, Si-FinFETs experience pronounced shifts in SS and V_T, with DIBL amplifying concurrently, signalling increased short-channel effects and weakened gate-channel coupling. The extreme SS deviation reaching 133.61 mV/dec at high temperature, compared to the ideal value of 54.6 mV/dec, emphasises the critical importance of thermal management in ultra-scaled transistor technologies.

Figure 12 illustrates the temperature-dependent variations in V_T, DIBL, and SS for the Si-FinFET device across temperatures of 275 K, 300 K, 325 K, and 350 K. A clear linear trend is observed over the examined temperature range: V_T decreases from 0.46 V to 0.41 V, SS increases from 89.67 mV/dec to 115.81 mV/dec, and DIBL rises from 34.71 mV/V to 48.45 mV/V, respectively.

Interestingly, the SS value at 275 K (89.67 mV/dec) represents the largest deviation from the ideal SS of 54.6 mV/dec. Despite this, 275 K also corresponds to the condition closest to the theoretical SS limit of 69.5 mV/dec, before SS continues to rise and peaks at 115.81 mV/dec at 350 K. This degradation in SS with temperature reflects the reduced gate control due to increased thermally generated carriers and interface trap activity.

In parallel, the observed increase in DIBL with temperature further indicates worsening short-channel effects and diminished electrostatic gate control. Collectively,

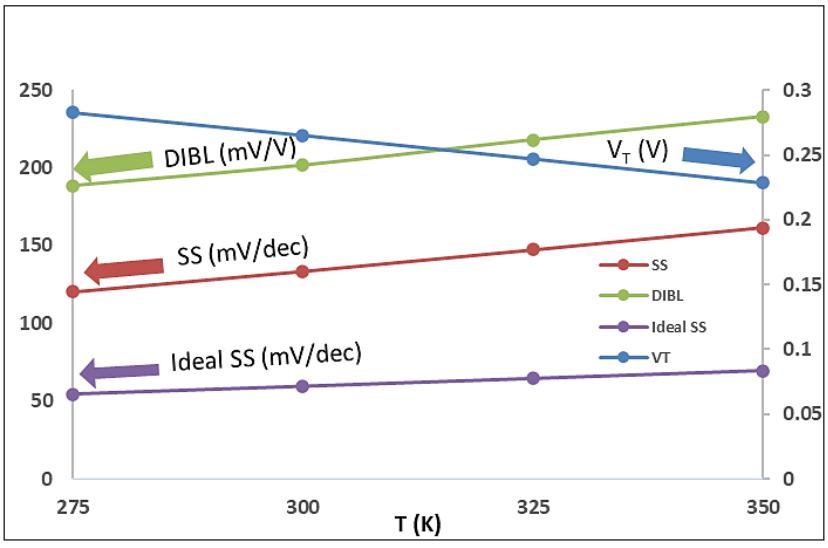

Figure 11. Plots of DIBL, SS, ideal SS, and V_T at Wg =10nm, Lg = 10nm

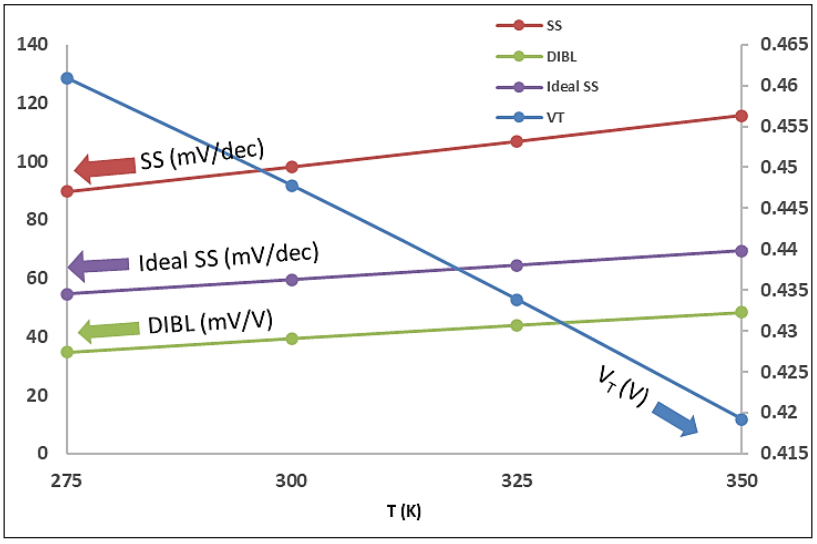

Figure 12. Plots of DIBL, SS, ideal SS, and V_T at W_g=10nm, L_g = 20 nm

these findings emphasise the thermally sensitive nature of FinFET parameters and the need for precise thermal management and design optimisation in advanced nanoscale devices.

Figure 13 elucidates the interrelationship between variations in DIBL, SS, V_T, and how these parameters evolve with temperature for a Si-FinFET device with gate length (L_g) of 20 nm across the range of 275 K to 350 K. A linear decrement in V_T is observed with increasing temperature, with V_T values reducing from 0.48 V at 275 K to 0.46 V at 350 K. Correspondingly, SS increases from 74.22 mV/dec to 99.93 mV/dec, while DIBL rises from 8.29 mV/V to 13.37 mV/V. The SS value of 74.22 mV/dec at 275 K deviates significantly from the ideal SS of 54.6 mV/dec, and this deviation becomes more pronounced at 350 K, where SS reaches 99.93 mV/dec, representing the furthest divergence from the theoretical optimum of 69.5 mV/dec. This degradation in SS reflects the deterioration of gate-channel control under thermal excitation, driven by enhanced carrier scattering and interface state activation. Simultaneously, the monotonic increase in DIBL with temperature highlights the exacerbation of short-channel effects and further reduction in electrostatic gate control. These findings confirm that as temperature rises, Si-FinFETs with L_g = 20 nm exhibit pronounced shifts in key electrical parameters, emphasising the critical influence of thermal variations on device performance and reliability.

Figure 14 presents the variations in V_T, SS, and DIBL as a function of Si-FinFET channel length at 300 K, with L_g incremented in 10 nm steps from 10 nm to 30 nm. As the channel length increases, SS exhibits a decreasing trend and approaches its ideal value at 30 nm, indicating improved gate control. Simultaneously, V_T demonstrates a gradual increase with channel length and eventually saturates, reflecting enhanced electrostatic stability.

Interestingly, DIBL shows a sharp peak at 10 nm, indicative of pronounced short-channel effects, and subsequently decreases with further scaling. These results suggest that a channel length range between 10 and 20 nm offers optimal performance under the investigated thermal conditions. Moreover, the linear correlation between channel length and the observed electrical properties reinforces previous findings reported by Hashim (2022b).

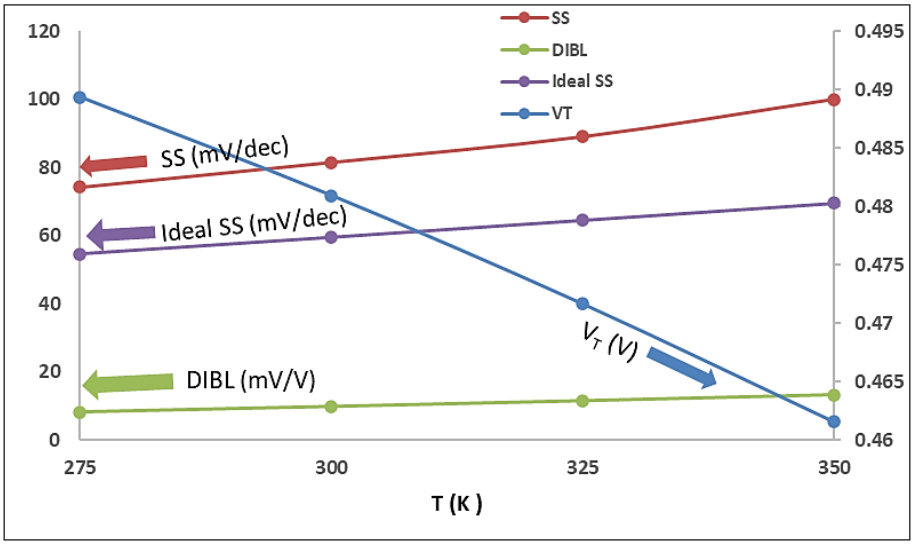

Figure 13. Plots of DIBL, SS, ideal SS, and V_T at W_g =10nm, L_g = 30 nm

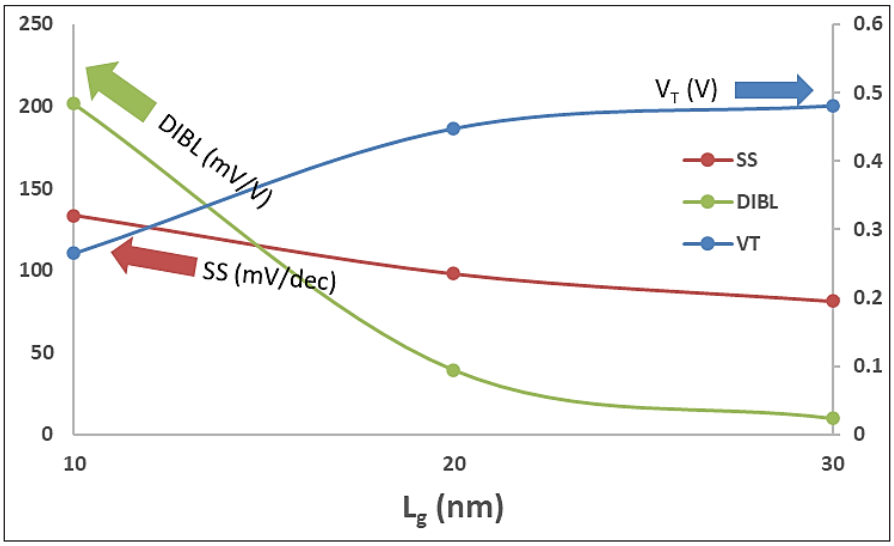

Figure 14. Plots of DIBL, SS and V_T with L_g

The dominant impact of temperature on Si-FinFET drain current is primarily attributed to enhanced carrier velocity in n-type Si-FinFETs as fin dimensions are scaled down. Remarkably, cross-sectional scaling of the channel exerts minimal influence on carrier velocity, underscoring the robustness of transport dynamics in ultra-scaled geometries. Furthermore, in aggressively downscaled MOSFETs, the drain saturation current is predominantly governed by the carrier injection velocity (V_{inj}) at the source-channel junction. Under ballistic transport conditions, this injection velocity, an intrinsic material property, becomes the primary determinant of drive current, superseding traditional mobility-limited conduction mechanisms (Yasir, 2024).

Table 1 provides a comparative overview of the most relevant prior studies and the present work. This comparison highlights key performance metrics of subthreshold swing (SS) and drain-induced barrier lowering (DIBL) across Si-FinFET devices with various gate lengths and fabrication approaches. The presented data underscore the improvements achieved in our study, particularly in terms of thermal stability and electrostatic control, while situating our findings within the broader context of existing literature.

Table 1
Comparison with other research works

Reference	Best Value of SS	Best Value of DIBL
Yu et al. (2002)	125 mV/dec	71mV/V
Liu et al. (2020)	80 mV/dec	10 mV/V
Jiang et al. (2009)	73 mV/dec	28mV/V
Jiang et al. (2009)	60 mV/dec	10 mV/V
Present study	89.6mV/dec	34.7mV/V

CONCLUSION

By systematically examining Si-FinFET channel lengths of 10, 20, and 30 nm, this study investigates the influence of temperature variations (275 K, 300 K, 325 K, and 350 K) on key device characteristics. Under diode-mode operation, extending the channel length up to 30 nm yields optimal increments in ΔI with respect to temperature; beyond this point, ΔI values stabilise, exhibiting minimal dependence on further channel length increases. At each temperature level, the behaviour of V_T, SS, and DIBL was analysed across the specified channel lengths. Notably, V_T exhibits a positive correlation with channel length, gradually increasing and approaching saturation beyond 20 nm. In contrast, SS decreases with increasing L_g, nearing the ideal theoretical value indicative of improved gate-channel coupling. Meanwhile, DIBL rises sharply at 10 nm, exhibits marginal growth at 20 nm, and begins to decrease at 30 nm, signifying a partial recovery in electrostatic integrity. Collectively, these findings suggest that the optimal channel length for Si-FinFET devices, under the thermal and electrical conditions considered in this study, lies within the 10 and 20 nm range.

This dimensional window strikes a favourable balance between thermal sensitivity, electrostatic control, and current modulation, making it ideal for nanoscale Si-FinFET-based temperature sensor applications.

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LIST OF ABBREVIATIONS

Si-FinFET	:	Silicon-based Fin Field-Effect Transistor
MuGFET	:	Multi-Gate Field-Effect Transistor
I-V	:	Current-voltage
MOSFET	:	Metal Oxide Field-Effect Transistor
FET	:	Field-Effect Transistor
BJT	:	Bipolar Junction Transistor
Si	:	Silicon
Ge	:	Germanium
GaAs	:	Gallium arsenide
InAs	:	Indium arsenide
DIBL	:	Drain-induced barrier lowering
V_T	:	Threshold voltage
SS	:	Sub-threshold swing
PDE	:	Partial differential equation
I_d	:	Drain current
V_g	:	Gate voltage
L_g	:	Gate length
W_g	:	Gate width
V_{DD}	:	Supply voltage
ΔI	:	Differential current
T	:	Temperature
V_{inj}	:	Injection velocity

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